

SN54HCT240, SN74HCT240 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCLS174B – MARCH 1984 – REVISED MAY 1997

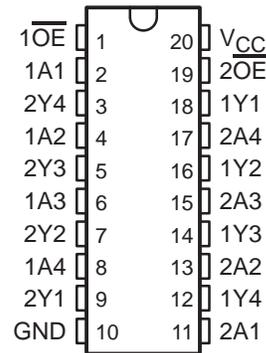
- Inputs Are TTL-Voltage Compatible
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- High-Current Outputs Drive up to 15 LSTTL Loads
- Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

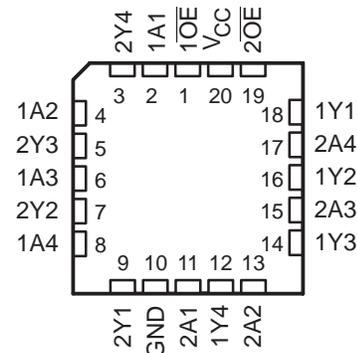
These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The 'HCT240 are organized as two 4-bit buffers/drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes inverted data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

The SN54HCT240 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HCT240 is characterized for operation from -40°C to 85°C .

SN54HCT240 . . . J OR W PACKAGE
SN74HCT240 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT240 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each buffer/driver)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	L
L	L	H
H	X	Z



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

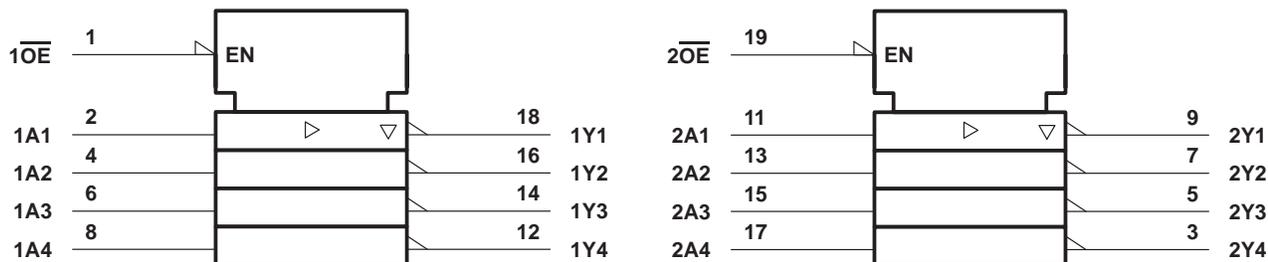
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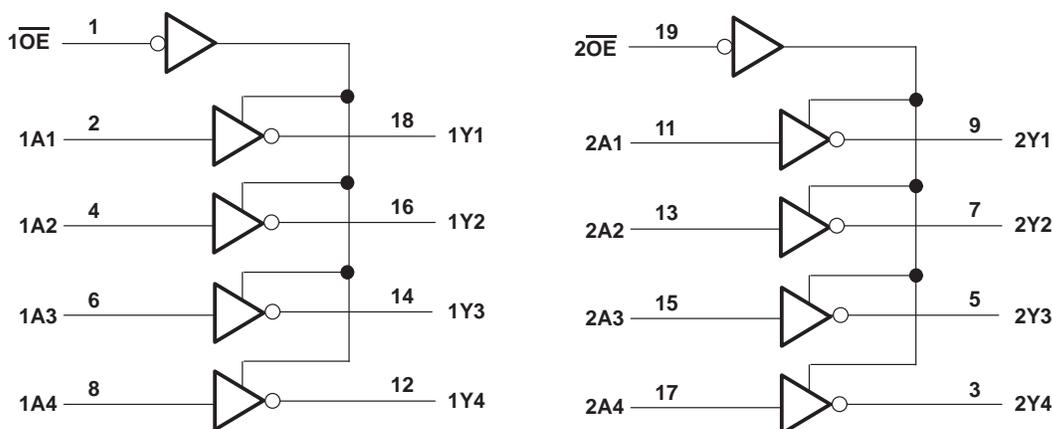
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND	± 70 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package	97°C/W
N package	67°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

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recommended operating conditions

		SN54HCT240			SN74HCT240			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		2	2		V	
V_{IL}	Low-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		0	0.8		V	
V_I	Input voltage	0		V_{CC}	0		V_{CC}	
V_O	Output voltage	0		V_{CC}	0		V_{CC}	
t_t	Input transition (rise and fall) time	0		500	0		500	ns
T_A	Operating free-air temperature	-55		125	-40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT240		SN74HCT240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	4.5 V	$I_{OH} = -20\ \mu\text{A}$		4.4	4.499	4.4	4.4	V	
			$I_{OH} = -6\ \text{mA}$		3.98	4.3	3.7	3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	4.5 V	$I_{OL} = 20\ \mu\text{A}$		0.001		0.1	0.1	V	
			$I_{OL} = 6\ \text{mA}$		0.17	0.26	0.4	0.33		
I_I	$V_I = V_{CC}$ or 0	5.5 V	± 0.1	± 100	± 1000	± 1000	nA			
I_{OZ}	$V_O = V_{CC}$ or 0, $V_I = V_{IH}$ or V_{IL}	5.5 V	± 0.01	± 0.5	± 10	± 5	μA			
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$	5.5 V	8		160	80	μA			
ΔI_{CC}^\dagger	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}	5.5 V	1.4	2.4	3	2.9	mA			
C_i		4.5 V to 5.5 V	3	10	10	10	pF			

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

switching characteristics over recommended operating free-air temperature range, $C_L = 50\ \text{pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT240		SN74HCT240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V	13	25	37	32	ns			
			5.5 V	12	23	33	29				
t_{en}	\overline{OE}	Y	4.5 V	21	35	53	44	ns			
			5.5 V	19	32	48	40				
t_{dis}	\overline{OE}	Y	4.5 V	19	35	53	44	ns			
			5.5 V	18	32	48	40				
t_t		Y	4.5 V	8	12	18	15	ns			
			5.5 V	7	11	16	14				



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switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$
(unless otherwise noted) (see Figure 1)

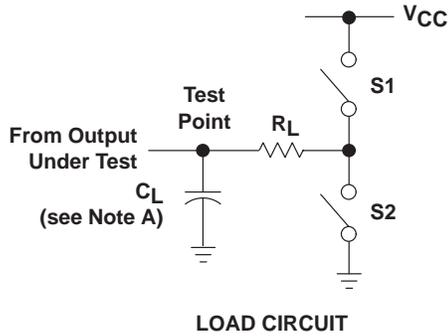
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT240		SN74HCT240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V	20	42	63	53	ns			
			5.5 V	19	38	56	48				
t_{en}	\overline{OE}	Y	4.5 V	25	52	79	65	ns			
			5.5 V	22	47	71	59				
t_t		Y	4.5 V	17	42	63	53	ns			
			5.5 V	14	38	57	48				

operating characteristics, $T_A = 25^\circ\text{C}$

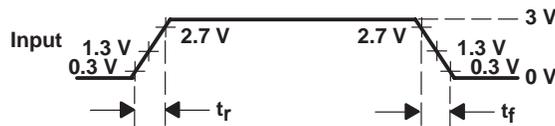
PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per buffer/driver	No load	40	pF



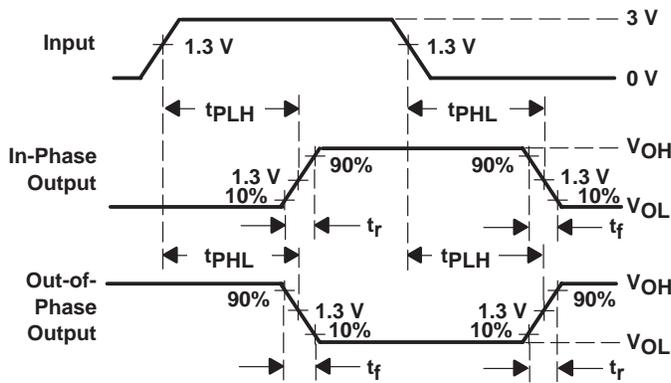
PARAMETER MEASUREMENT INFORMATION



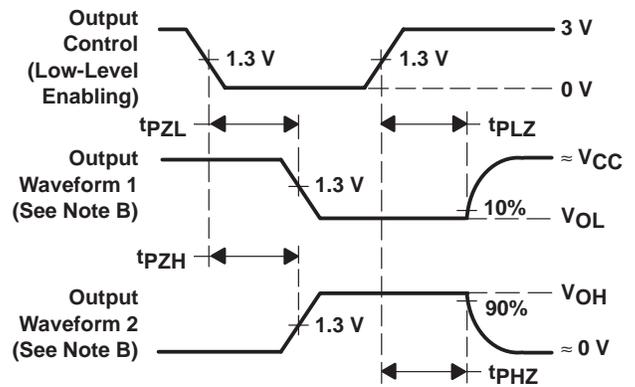
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 k Ω	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 k Ω	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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