Overview for Today

- Binary addition: recap and complete
  - Truth table
  - Half adder and full adder circuits
- Video
  - Initial uses for computers
  - Tubes to transistors
- Memory circuits
  - Feedback

Recap: Binary Numbers

- Physical representation
  - Concept of “on” and “off” for physical manufacturing of computers
  - Transistor
- Abstract representation
  - Propositional logic: AND, OR, NOT
  - Boolean algebra
- ANY Boolean expression can be built with transistors
Recap: Transistors

Recap Logic Gate: AND Function

Recap Logic Gates: Symbols

Recap Logic Functions: AND, OR

- Two inputs, one output
- The ‘AND’ and ‘OR’ functions

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>AND (+)</th>
<th>OR (+)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
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<td>1</td>
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<td>0</td>
<td>1</td>
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<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

- This is a truth table
Onto the Adder Circuit...

Binary Addition: Half Adder

- We need a circuit to add two bits
  - Either bit can be ‘0’ or ‘1’
- The function in the truth table is
  - $\text{Sum} = A'B + AB' \Rightarrow \text{Exclusive-OR function}$
  - $\text{Carry} = AB$

<table>
<thead>
<tr>
<th>$A$</th>
<th>$B$</th>
<th>Sum</th>
<th>Carry</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
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</table>

Binary Addition

- Adding decimal numbers
  - Concept of the carry digit
  - 15
  - 27
  - 42
- Adding binary numbers
  - Concept of sum and carry bits
The Half-Adder and Exclusive OR Gate

• A’B + AB’ = Exclusive OR
  – Typically abbreviated to XOR
  – Simulator uses EOR

```
\begin{align*}
\text{S} &= x \oplus y \\
\text{C} &= xy \\
\end{align*}
```

Binary Addition: Full Adder

• A full adder is a circuit has *three* inputs (including a ‘carry-in’) and two outputs (the sum and carry-out)
  – What is the third input?
  – Exercise: Add $111 + 101$

```
\begin{array}{c}
\text{Cin} \\
1 & 1 & 1 \\
1 & 0 & 1 \\
1 & 1 & 1 \\
\end{array}
```

• Cascade two halfadders to get a full adder

• For adding two numbers, we need three inputs
HW: Cascade 2 Full Adders for a 2-Bit Adder

\[ A_2 A_1 \oplus B_2 B_1 = 11 + 10 \]

**Memory Circuits & Feedback**

**Design Criteria for Memory?**

- A large array of all memory locations
  - Each location stores multiple-bits
    - 8 bits, 16 bits, 32...
- Each location has a unique (binary) address

** Memory “Array” **

** The data bus is shared by all storage locations (all addresses) **

- Implications of this?
Memory Array Construction

- Build a 1-bit memory cell (binary cell or ‘BC’)
- Cascade 1-bit cells to the ‘word’ size desired
  - Word = 4 bits in class examples
  - Word = 64 bits on new Pentiums
- Include control lines
  - Select: to select desired location/address
  - Read/write: either read or write from/to the location
- Include data bus
  - The data bus will have as many lines as there are bits in the word (e.g., 4 here, 64 in the Pentium)
The Concept of Feedback

- The output of a circuit becomes (is fed-back to) one of the inputs
- Important category of circuits for which looking at the inputs does not tell you the value of the output
- §2.3, page 58 on

1-Bit Memory Circuit

- Memory circuit
  - Has two possible states, ‘1’ and ‘0’
  - The circuit stores or remembers the state
  - If we can control which value is stored (and we have the means to read this value), then we have a memory (RAM) circuit

Problems With Simple Memory Circuit

- Having two inputs is cumbersome
- We do not have good control over when (under what conditions) data is stored or read
  - Each cell must be read or written to only when its unique address is selected

1-Bit Memory: Load Control

[Diagram of 1-Bit Memory Circuit]
1-Bit Memory: R/W, Select, Data Bus

Behavior of 1-Bit Memory Cell

- When select = 0, nothing happens (the cell is inactive)
- When select = 1 and read/write = 0, a copy of the stored bit is put on the data bus (reading from the cell)
- When select = 1 and read/write = 1, the data on the data bus is stored into the cell (writing to the cell)

Cascaded 1-Bit Memory Cells

Memory Array
Summary

- Binary addition
  - Half adder and full adder circuits
  - Cascading circuits to make larger ones
- Memory
  - 1-bit storage & feedback
  - Control lines: R/W and select (address)
  - Data bus

Administration

- Quiz 1 – posted for due at midnight Thursday. Late getting up, so due by 4pm Friday
- TA – but not for HW 2 (for subsequent work)