Outline

Homework 2 (feedback)

Decoders, Cascading Decoders

Multiplexers

Journey into Mystery
Review Homework 2

- **Problem 1**: AND with inverted input: universal!

- **Problem 2**:
  - $g(a,b,c,d)$ can be verified using M11
  - $\Pi(x,x,x,x)$ shows 0s in Karnaugh maps, not 1s
  - Use largest covers possible

- **Problem 3**:
  - Active-low signals should have a circle on them

- **Problem 4**:
  - Simplicity wins!
Python Decoder

```python
def decoder( enable, a, b, c):
    L = 8*[0]
    if enable==1:
        decimal = c + b*2 + a*4
        L[decimal] = 1
    return L
```

http://www.science.smith.edu/dftwiki/index.php/3-to-8_Decoder_in_Python
Outline

Homework 2 (feedback)

Decoders, Cascading Decoders

Multiplexers

Journey into Mystery
3-to-8 with 2-to-4s?

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Outline

Homework 2 (feedback)

Decoders, Cascading Decoders

Multiplexers

Journey into Mystery
Multiplexers
4-to-1 Mux
4-to-1 Mux

(Mechanical Analogy)
4-to-1 Mux

(Mechanical Analogy)
4-to-1 Mux

(Mechanical Analogy)
4-to-1 Mux

(Mechanical Analogy)
What logic circuit will we find inside the Mux?

4-to-1 Mux

I_0
I_1
I_2
I_3

C_0
C_1
Y
8-INPUT MULTIPLEXER

The TTL/MSI SN54/74LS151 is a high speed 8-input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. The LS151 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

- Schottky Process for High Speed
- Multifunction Capability
- On-Chip Select Logic Decoding
- Fully Buffered Complementary Outputs
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)

PIN NAMES

VCC = PIN 16
GND = PIN 8
\( \otimes \) = PIN NUMBERS
A Memory Chip

Figure  Organization of a 1K x 1 memory chip.

http://www.slideshare.net/binbinno/memory-systems-n
**Mux as Generic Building Block: Exercise 1**

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<th>01</th>
<th>11</th>
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![Diagram](image)
Mux as Generic Building Block: Exercise 2

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FOOL! DID YOU THINK YOU COULD ESCAPE US??

YOU'VE NEVER READ A TALE LIKE "THE SORCERER!"

GO BACK! BACK TO THE DARK WORLD FROM WHENCE YOU COME! BEGONE! I COMMAND YOU!

D. Thiebaut, Computer Science, Smith College
What does **Combinational** Mean?

Is $f(a,b)$ always predictable? Always deterministic?
How does this work?

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q1</th>
<th>Q2</th>
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<tbody>
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(Demo starts around 1min 52sec)

https://www.youtube.com/watch?v=mo4Lq0DvJ68
We stopped here last time…
The RS Latch

- \( R = \text{Reset}, \ S = \text{Set}, \ Q = \) usual name for the output of a circuit that has a “state”
- The circuit has a feedback loop
- The circuit has a state
The RS Latch Explained

\[ S \rightarrow Q_1 \]
\[ R \rightarrow Q_2 \]
The RS Latch Explained

\[ S \quad Q_1 \]
\[ Q_2 \quad R \]
Ouroboros

From Wikipedia, the free encyclopedia

For other uses, see Ouroboros (disambiguation).

The ouroboros or uroboros (/ˈɔːroʊboʊrəs, ɔːroʊˈboʊrəs/,[3] from the Greek οὐροβόρος ὄφις tail-devouring snake) is an ancient symbol depicting a serpent or dragon eating its own tail.
The RS Latch Explained

\[ S \rightarrow Q_1 \rightarrow Q_2 \rightarrow R \]
The RS Latch Explained

\[ S \quad Q_1 \quad 1 \]
\[ Q_2 \quad R \quad 0 \]

Diagram: RS latch circuit with inputs S and R, and outputs Q1 and Q2.
The RS Latch Explained

S → Q1
Q2 → R

0 1
The RS Latch Explained

S \rightarrow Q_1
Q_2 \rightarrow R

0 \rightarrow Q_2
1 \rightarrow Q_1
The RS Latch Explained

![RS Latch Diagram]
The RS Latch Explained
The RS Latch Explained
The RS Latch Explained

1

Q_2

0

Q_1

S

R
The RS Latch Explained

\[ \text{S} \quad \text{Q}_1 \quad \text{R} \]

1

Q_2

0
The RS Latch Explained

[Diagram showing the RS latch with gates and inputs S, Q2, and R connected to Q1 and 0 and 1 values]
The RS Latch Explained

RS Latch Diagram:
- **S** (Set) input
- **R** (Reset) input
- **Q1** and **Q2** outputs
- Switch positions:
  - **0** for Reset
  - **1** for Set

Visual representation:
- **Yellow arrow** indicating state transition
The RS Latch Explained
The RS Latch Explained

\[ S \quad Q_1 \quad 1 \]
\[ Q_2 \quad R \]
Latch = Sequential Circuit

R
S
Q1
Q2
time
time
time
time
Important Properties of the Latch

- Gates must have ability to pass and to block
- There must be a loop
- There must be two inversions in the loop
Concepts of Passing and Blocking

\[ \begin{align*}
    & 1 & \quad & a & \quad & a' \\
    & a & & & & \\
    & 1 & & & &
\end{align*} \]

\[ \begin{align*}
    & 0 & \quad & a & \quad & 1 \\
    & a & & & & \\
    & 0 & & & &
\end{align*} \]

\[ \begin{align*}
    & 0 & \quad & 1 & \quad & 1 \\
    & 0 & & & & \\
    & 0 & & & &
\end{align*} \]

\[ \begin{align*}
    & 0 & \quad & 0 & \quad & 1 \\
    & 0 & & & & \\
    & 0 & & & &
\end{align*} \]
Concepts of Passing and Blocking

\[ \begin{array}{cc}
\text{a} & \text{a'} \\
0 & 1 \\
1 & 0 \\
\end{array} \]
Improving on the RS Latch
Can do even better!
Meet the D-Flip-flop!

**DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP**

The SN54/74LS74A dual edge-triggered flip-flop utilizes Schottky TTL circuitry to produce high speed D-type flip-flops. Each flip-flop has individual clear and set inputs, and also complementary Q and Q outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or the LOW level, the D input signal has no effect.

**MODE SELECT — TRUTH TABLE**

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<thead>
<tr>
<th>OPERATING MODE</th>
<th>S_D</th>
<th>S_D</th>
<th>D</th>
<th>Q</th>
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<tbody>
<tr>
<td>Set</td>
<td>L</td>
<td>H</td>
<td>X</td>
<td>H</td>
<td>L</td>
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<tr>
<td>Reset (Clear)</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>L</td>
<td>H</td>
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<tr>
<td>Undetermined</td>
<td>L</td>
<td>L</td>
<td>X</td>
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<tr>
<td>Load &quot;1&quot; (Set)</td>
<td>H</td>
<td>H</td>
<td>h</td>
<td>H</td>
<td>L</td>
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<tr>
<td>Load &quot;0&quot; (Reset)</td>
<td>H</td>
<td>H</td>
<td>i</td>
<td>L</td>
<td>H</td>
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</table>

Both outputs will be HIGH while both S_D and C_D are LOW, but the output states are unpredictable if S_D and C_D go HIGH simultaneously. If the levels at the set and clear are near V_{IL} maximum then we cannot guarantee to meet the minimum level for V_{OH}.

H, h = HIGH Voltage Level
L, i = LOW Voltage Level
X = Don't Care

Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

**ORDERING INFORMATION**

- SN54LSXXJ Ceramic
- SN74LSXXN Plastic
- SN74LSXXD SOIC

**LOGIC SYMBOL**

- VCC = PIN 14
- GND = PIN 7

**SN54/74LS74A**

- J SUFFIX CERAMIC CASE 632-08
- N SUFFIX PLASTIC CASE 646-06
- D SUFFIX SOIC CASE 751A-02
Meet the D-Flip-flop!

When a latch becomes "edge-triggered" we call it a Flip-flop.
Preparation for Lab 4
Definitions

\[ T = \text{Period} \] (measured in ms, us, ns)

\[ \text{Frequency} = \frac{1}{T} \] (1/ms=kHz, 1/us=MHz, 1/ns=GHz)

Amplitude (Volts)
We stopped here last time…