1) Simply create a voltage divider and put the resistor to measure in series with a 10kΩ resistor. Measure $V_1$ and $V_2$

$$R = \frac{V_2}{I} \quad \{ \begin{align*}
R &= \frac{V_2}{I} \\
I &= \frac{V_1}{10kΩ}
\end{align*} \}$$

If you measure $V_1$ only, then $R = \frac{(5 - V_1)}{V_1}$ x 10kΩ

2) a b 00 01 11 10

\[ \text{Diagram of a 4-bit counter with inputs a and b.} \]

\[ \text{Diagram of a 4-bit decoder with inputs a, b, and c.} \]

\[ \text{Diagram of a 4-to-1 multiplexer with inputs a and b.} \]

Note: Do not forget the active-low enable.

Indicate the name of the signals. I prefer the solution that used only one of the two multiplexers, although the other solution is ok, though more expensive.
3. \( c = a \cdot b \quad s = a + b \)

3) The circuit can be neither be set, nor reset. It is not a latch. Make sure that when you are asked if something is one thing, a not, that you actually write "Yes, it is \( \times \)" or "No, it is not a \( \times \)."

4) The first function
\[ f = \overline{b} \cdot d + b \cdot \overline{d} \]
⇒ we should use \( \overline{b} \cdot d \) for selection. ⇒ No additional gate needed!

5) 8 states \( \Rightarrow 2^3 = 8 \)
2 flipflops needed.
\[ C = \overline{Q_2} + \overline{Q_1} \overline{Q_0} \]
\[ Y = Q_2 Q_1 Q_0 \]
\[ R = \overline{Q} \]

Note that
\[ K = \overline{G} \]
we can use this to simplify our design.

Use Karnaugh maps to generate
\( D_0, D_1, \) and \( D_2 \)

Equation:
\[ D_2 = \overline{Q_0} Q_1 + \overline{Q_0} Q_2 \]
\[ D_1 = Q_0 \overline{Q_2} + \overline{Q_0} Q_1 \]
\[ D_0 = \overline{Q_2} + Q_0 \]

Diagram: A logic circuit diagram showing the connections between inputs and outputs, with Gates and logic levels indicated.

Clock and preset inputs: All clock and preset inputs connected to 1 (5V).