1) \[ z(A, B, C, D) = \Sigma(0, 1, 2, 3, 12, 13, 14, 15) \]

The function inputs C and D don't need to be connected to the 74LS153 to implement z. Many of the inputs of the 74LS153 aren't needed to implement z, so it doesn't matter what they are connected to (indicated by the X), and we aren't interested in the output they generate (Zb).

2) State diagram:

\[
\begin{array}{c|c|c|c|c}
S^n & S^{n+1} \\
\hline
S_0 & S_1 & S_2 & S_3 \\
000 & 001 & 011 & 010 \\
\hline
S_7 & S_6 & S_5 & S_4 \\
100 & 101 & 111 & 110 \\
\hline
\end{array}
\]
Other tables:

<table>
<thead>
<tr>
<th>$Q_2Q_1Q_0^n$</th>
<th>$Q_2Q_1Q_0^{n+1}$</th>
<th>$Q_2Q_1Q_0$</th>
<th>G</th>
<th>Y</th>
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Equations for $D$ inputs:

- $D_2 = Q_1.Q_0' + Q_2.Q_0$
- $D_1 = Q_2'.Q_0 + Q_1.Q_0'$
- $D_0 = (Q_2 \oplus Q_1)'$

Equations for $G$, $Y$, $R$ signals:

- $G = Q_2' + Q_1.Q_0'$
- $Y = Q_1.(Q_2' + Q_0')$
- $R = Q_2.(Q_0 + Q_1')$

Diagram:
3) This circuit is not a latch. Whenever the output of the NAND gate is 1 (and the output of the NOR gate is 0), the circuit gets stuck with those outputs. No matter how the inputs are changed, Q_i stays at 0 and Q_j stays at 1. Since there is no way to switch the outputs, the circuit cannot be a latch.