



# Circuit design on CPLD chips using Verilog

Tiffany Q. Liu

Faculty advisor: Dominique F. Thiébaud  
Department of Computer Science  
Smith College

## Objective

**GOAL:** replace Heathkit wiring of circuits used in CSC 270 Digital Circuits and Systems with CPLD kit programmed in Verilog.

**REQUIREMENTS:** provide the ability to program adders, multiplexer-based circuits, Moore-style flip-flop sequencers, and ROM-based sequencers.

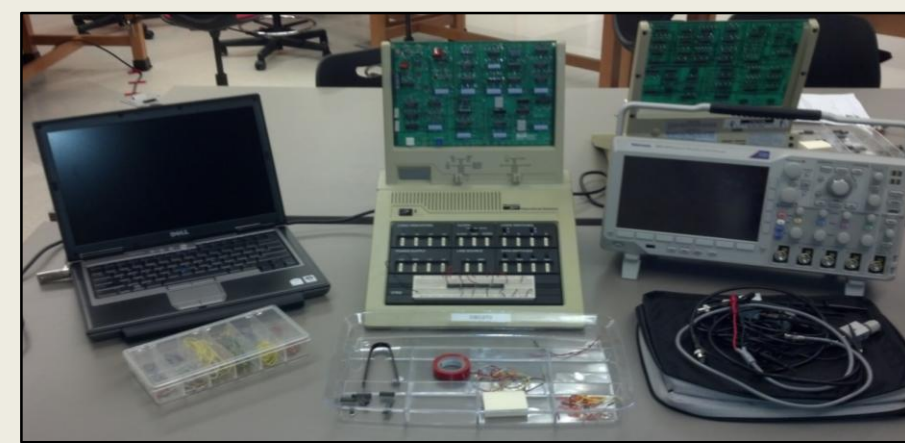


Fig. 1. CSC 270 lab bench pre-Fall 2011.



Fig. 2. CSC 270 lab bench post-Fall 2011.

## Background

**CPLD:** Complex Programmable Logic Device, design independent integrated circuit.

**Advantages:** users can design more complicated circuit systems in a more time and cost efficient manner.

**Verilog:** standardized and vendor independent hardware description language used to write code for circuit synthesis and simulation.

Trivia: What's the difference between a CPLD and a FPGA?

CPLD	FPGA
10 <sup>3</sup> -10 <sup>4</sup> logic blocks	10 <sup>4</sup> -10 <sup>6</sup> logic blocks
Non-volatile memory	RAM-based memory
Simpler to design	More flexible

## Recreated Lab Exercises

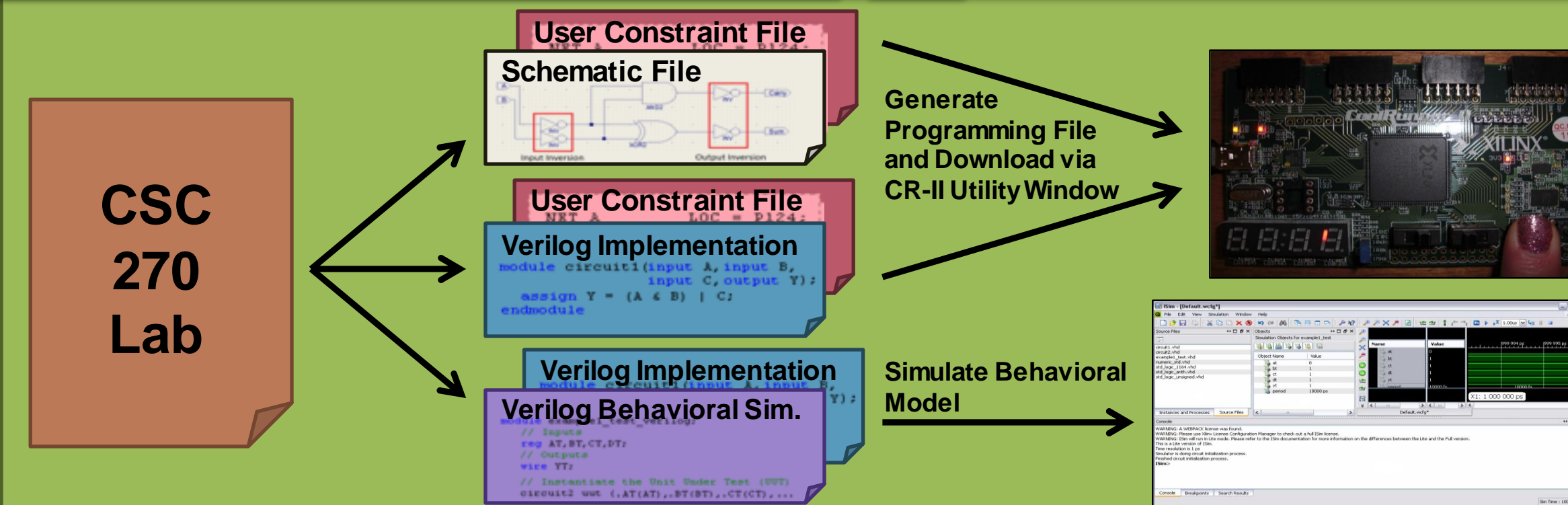


Fig. 3. CSC 270 labs are recreated using three different methods: *Schematics, Verilog Implementation, and Verilog Behavioral Simulation.*

Using Verilog, traffic light sequencer can be programmed using a *clocked always block and case structure.*

Directly copied wiring diagram into Schematic file.

**CSC 270 Traffic Light Sequencer Diagrams**

Present	Future	Output	
S <sub>n</sub>	Q <sub>n</sub> <sup>0</sup> Q <sub>n</sub> <sup>1</sup> Q <sub>n</sub> <sup>2</sup>	Q <sub>n+1</sub> <sup>0</sup> Q <sub>n+1</sub> <sup>1</sup> Q <sub>n+1</sub> <sup>2</sup>	G Y R
S <sub>0</sub>	0 0 0	1 S <sub>1</sub>	0 0 1
S <sub>1</sub>	0 1 1	1 S <sub>2</sub>	1 0 0
S <sub>2</sub>	1 0 0	0 S <sub>0</sub>	0 1 0
S <sub>3</sub>	1 1 1	1 S <sub>0</sub>	0 0 1

```

always
//State 0 (G*Y* active low) --> State 1 (G*Y* active low)
//State 1 (G*Y* active low) --> State 2 (G*Y* active low)
//State 2 (G*Y* active low) --> State 0 (G*Y* active low)
//State 3 (G*Y* active low) --> State 3 (G*Y* active low)
case (state)
  00: begin
    state <- 01;
    G = 1;
    Y = 0;
    R = 1;
  end
  01: begin
    state <- 10;
    G = 0;
    Y = 1;
    R = 1;
  end
  10: begin
    state <- 00;
    G = 1;
    Y = 0;
    R = 1;
  end
  11: begin
    state <- 11;
    G = 0;
    Y = 0;
    R = 1;
  end
endcase

```

**Traffic Light Sequencer Signals Generated via ISim:**

Fig. 4. Sample recreated lab for a traffic light sequencer that cycles from red to green to yellow and back or that remains red.

## Hardware + Software Kit



## Final Outcome

Designed a *collection of labs/tutorials that is tailored to CSC 270 students or students of similar levels learning how to create simple combinational circuits and sequential circuits using Verilog and CPLDs.*

## References

- 1 Palnitkar, S. (1996). *Verilog HDL: A guide to digital design and synthesis*. Upper Saddle River: SunSoft Press.
- 2 Smith, D.J. (1996). *HDL chip design: A practical guide for designing, synthesizing and simulating ASICs and FPGAs using VHDL or Verilog*. Madison: Doone Publications.
- 3 *Xilinx ISE Simulator (ISim) with Verilog Test Fixture Tutorial*. (2010). Retrieved November 12, 2011 from [http://digilentinc.com/Data/Documents/Tutorials/Xilinx ISE Simulator \(ISim\) with Verilog Test Fixture Tutorial.pdf](http://digilentinc.com/Data/Documents/Tutorials/Xilinx ISE Simulator (ISim) with Verilog Test Fixture Tutorial.pdf)
- 4 *Xilinx ISE WebPACK Schematic Capture Tutorial*. (2010). Retrieved November 12, 2011 from <http://digilentinc.com/Data/Documents/Tutorials/Xilinx ISE WebPACK Schematic Capture Tutorial.pdf>
- 5 *Xilinx ISE WebPACK Verilog Tutorial*. (2010). Retrieved November 12, 2011 from <http://digilentinc.com/Data/Documents/Tutorials/Xilinx ISE WebPACK Verilog Tutorial.pdf>

## Acknowledgements

This project was funded by the *Smith College Department of Computer Science*. Special thanks to *Professor Dominique F. Thiébaud* for his support and for providing the opportunity and means of working on this project.

## For further information

Please contact [tliu@smith.edu](mailto:tliu@smith.edu). More information on this and the recreated lab exercises and tutorials can be obtained at <http://bit.ly/xRz618>.