Circuit design on CPLD chips using Verilog

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The goal of this independent study project was to port the digital design labs in CSC 270 *Digital Circuits and Systems* from wiring circuits on *Heathkit* breadboards to programming the same logic on a Xilinx *Complex Programmable Logic Device* (CPLD).

Now students can design circuit systems such as adders, multiplexer-based circuits, Moore-style flip-flop sequencers, and ROM-based sequencers by programming in *Verilog* instead of using physical wires and chips. Programming CPLDs allows users to design more sophisticated circuits in a more time and cost efficient manner.

Using the CoolRunner-II CPLD ($54) and the Xilinx ISE Design Suite (free) installed on a computer running Windows 7, I ported all the labs to Verilog and CPLD. Each laboratory exercise was recreated using three different methods: *Schematics*, *Verilog Implementation*, and Verilog *Behavioral Simulation*.

The CPLD and the Xilinx ISE Design Suite made designing and testing circuits more portable. I can design the circuit, test the circuit, and generate the signals with just the CPLD, a USB connector, and a laptop. The most significant difference that can be seen between using physical wires and chips and programming the CPLD was with the Traffic Light Sequencer Lab. Using Verilog, the traffic light sequencer can be programmed with a *clocked always block* and a *case structure*. From a programmer's approach to the problem, using this syntax was more intuitive than wiring flip-flops and logic gates.

At the conclusion of this independent study, I have designed a collection of labs and tutorials that is tailored to second-year computer science majors who can nowdesign simple combinational and sequential circuits in Verilog, on a laptop connected to a CPLD.