Circuit design on CPLD chips using Verilog

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Objective

GOAL: replace Heathkit wiring of circuits used in CSC 270 Digital Circuits and Systems with CPLD kit programmed in Verilog.

REQUIREMENTS: provide the ability to program adders, multiplexer-based circuits, Moore-style flip-flop sequencers, and ROM-based sequencers.

Fig. 1. CSC 270 lab bench pre-Fall 2011.

Fig. 2. CSC 270 lab bench post-Fall 2011.

Background

CPLD: Complex Programmable Logic Device, design independent integrated circuit.

Advantages: users can design more complicated circuit systems in a more time and cost efficient manner.

Verilog: standardized and vendor independent hardware description language used to write code for circuit synthesis and simulation.

Trivia: What's the difference between a CPLD and a FPGA?

CPLD	FPGA
10^3-10^4 logic blocks	10^4-10^6 logic blocks
Non-volatile memory	RAM-based memory
Simpler to design	More flexible

Recreated Lab Exercises

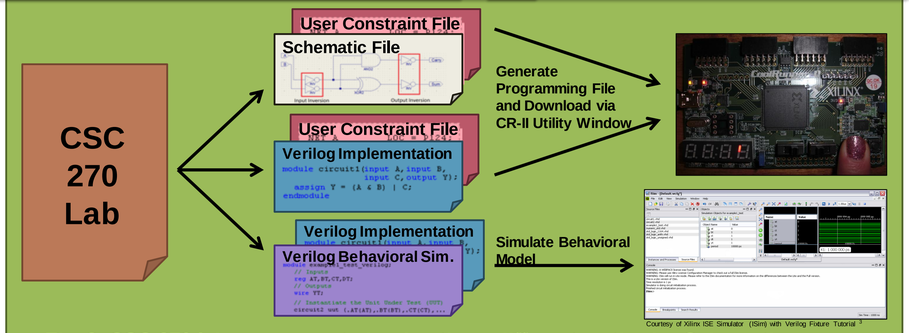


Fig. 3. CSC 270 labs are recreated using three different methods: *Schematics*, *Verilog Implementation*, and *Verilog Behavioral Simulation*.

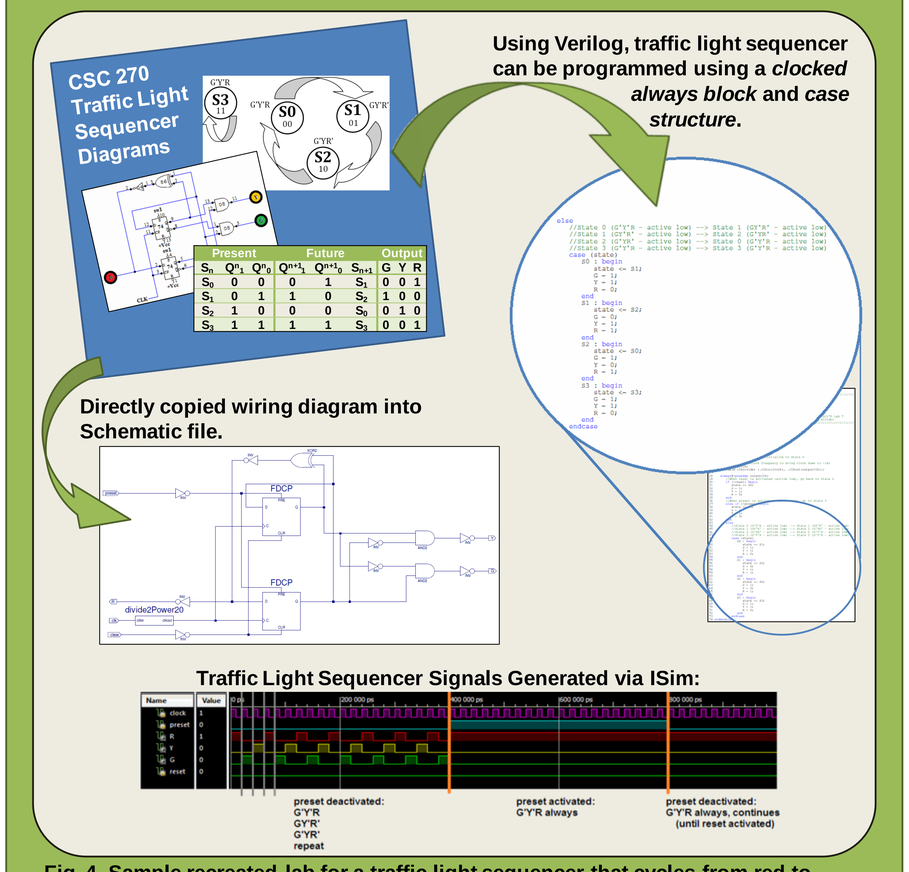
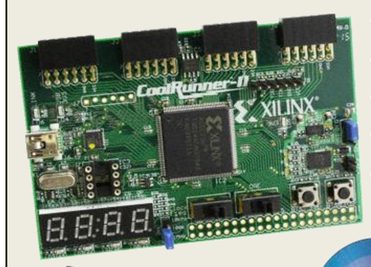


Fig. 4. Sample recreated lab for a traffic light sequencer that cycles from red to green to yellow and back or that remains red.

Hardware + Software Kit



- **CoolRunner-II CPLD**
- **USB connector**
- **XILINX® ISE Design Suite**
- **CoolRunner-II Utility Window**
- **Computer with Windows OS**

Final Outcome

Designed a *collection of labs/tutorials that is tailored to CSC 270 students or students of similar levels learning how to create simple combinational circuits and sequential circuits using Verilog and CPLDs*.

References

[1] **Palnitkar, S. (1996). *Verilog HDL: A guide to digital design and synthesis*. Upper Saddle River: SunSoft Press.**

[2] **Smith, D.J. (1996). *HDL chip design: A practical guide for designing, synthesizing and simulating ASICs and FPGAs using VHDL or Verilog*. Madison: Doone Publications.**

[3] **Xilinx ISE Simulator (ISim) with Verilog Test Fixture Tutorial. (2010). Retrieved November 12, 2011 from http://digilentinc.com/Data/Documents/Tutorials/Xilinx ISE Simulator (ISim) with Verilog Test Fixture Tutorial.pdf**

[4] **Xilinx ISE WebPACK Schematic Capture Tutorial. (2010). Retrieved November 12, 2011 from http://digilentinc.com/Data/Documents/Tutorials/Xilinx ISE WebPACK Schematic Capture Tutorial.pdf**

[5] **Xilinx ISE WebPACK Verilog Tutorial. (2010). Retrieved November 12, 2011 from http://digilentinc.com/Data/Documents/Tutorials/Xilinx ISE WebPACK Verilog Tutorial.pdf**

Acknowledgements

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For further information

Please contact *tliu@smith.edu*.
More information on this and the recreated lab exercises and tutorials can be obtained at *http://bit.ly/xRz618*.